**Project Description**

With the advancement of biomedical electronics, demand for ultra-low power integrated circuits is increasing day by day. As a very important block in biomedical sensors & wireless monitoring technology, the phase locked loop (PLL) is still one of the most power-consuming parts of the system. Therefore, it is very desirable to design and implement PLLs with very low power consumption overcome problems common at low power levels, such as, high supply noise sensitivity.

A typical radio-frequency (RF) PLL consists of the following blocks – a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF) and a frequency divider. Figure 1 shows the block diagram of a typical PLL. Among these blocks, the VCO and the divider are the most power-consuming blocks [1]. To reduce power requirement of the PLL, optimal low-power design is required for these two blocks.

![Block diagram of a typical Phase Locked Loop.](image)

In this design, we’ve set a target of 12 µW total power consumption for a PLL, which will be functioning as a frequency synthesizer for a MICS-band transmitter. This power budget is sufficient for many biomedical applications, such as energy-harvesting, implantable wireless sensors.

For the VCO block in this PLL, a ring oscillator is used due to its low power consumption. The oscillator consists of three minimum-sized inverters to reduce its current requirement. The oscillator frequency is controlled through current starving. Power consumption of 2.5 µW has been determined by simulation. Figure 2 shows the topology of the oscillator block.

![Current-starved ring oscillator topology.](image)

For the frequency divider block, a high frequency prescaler using TSPC logic and a low frequency static-logic divider have been used to reduce power requirement. Power consumption is also minimized through the use of minimum size MOSFETs. The divide ratio can be varied from 15 to 31744 with external digital control. Simulation shows 5 µW power requirement for the entire divider block with divide ratio of 12500, which is required for the PLL to run at 400 MHz from a 32 kHz reference. The other blocks, such as PFD,
current-output CP, LF and other auxiliary blocks, are based on conventional topologies and consume a total of 4 µW.

**Measurement Results**

Agilent™ DSO7034B Oscilloscope and Agilent™ N9010A Signal Spectrum Analyzer are employed to test the circuits. Figure 3 shows the test setup for the designed PLL. Chip-on-board bonding has been used to avoid the lead inductance and capacitances of packaging. The test board along with circuitry for regulated 1-V supply from battery has been placed inside a metal box. An on-chip current reference based on the design in [2] has been used to achieve low supply sensitivity.

The PLL output is obtained through an on-chip digital buffer, capable of driving 20pF capacitance at 400MHz with full-rail 1V swing. In measurement, the output is actually of very low power and contains large amount of noise. Figure 4 shows the output of the PLL in the Spectrum Analyzer.
Figure 4: Spectrum of PLL output through a digital buffer. The blue line is the real-time spectrum of the output. The yellow line is the record over time of the variation of center frequency of the PLL with time. This output contains large amount of noise.

Figure 5 shows the tuning voltage of the VCO of the PLL. It is seen that the tuning voltage is oscillating, which should be the dominant source for the noise in the PLL output spectrum. In normal 400MHz operation, this tuning voltage should be stabilizing to 0.5 V. Further investigation is needed to manipulate the loop dynamics of the PLL and remove the oscillation in the tuning voltage such that a cleaner spectrum is obtained from the PLL. This includes varying the gate-voltage of the transistor which acts as a resistance in the third-order LF (as shown in Figure 6) of PLL.

Figure 5: Tuning voltage for VCO generated from PFD, CP and LF blocks in PLL. The tuning voltage should be stabilizing to 0.5V for 400MHz PLL operation.
Power consumption of PLL has been measured to be approximately 30 µW from 1V power supply.

**Fabrication Process**

The **IBM 90nm 9LP/RF** CMOS process run on June 13, 2011 offered through MOSIS was used for fabricating the proposed circuits.

**Project Size**

The used chip area is **4 mm x 4 mm or 16 mm²**.

**Packaging**

We used **OCP_LQFP64A** for packaging the chip through MOSIS.

**Testing**

The fabricated chip is being tested in the Integrated Silicon Systems Laboratory of The University of Tennessee, Knoxville.

**References**
