Report of the final project (4 bit counter design) for ECE 533

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Introduction:

The project was to design a 4 bit counter with appropriate flipflop in cadence. For this project schematic, layout of the 4 bit counter was done, Design rule check(DRC) was done to check any error and LVS(layout vs schematic) was done to check if the schematic and layout match. It provided a great opportunity to work in cadence and to build all the basic building blocks(basic gates) and to design the counter based on those building blocks. The performance of the counter was checked for different loads and different characteristic parameters like rise time, fall time and propagation delay were measured for different loading effects.

The design steps:

The central part of the design was the design of a D Flip Flop. For this a master slave D flip flop was used in this project. D Flip-Flop is widely used as a flipflop and it is easier to use. It has one input and with the master slave approach it avoids any glitch. Also the design for the counter is well suited for D flip flop. So the choice of the d flip flop is justified.

To design the D Flipflop 8 Nand gates were used with one inverter. No library was allowed so basic Nand gates and Inverter was designed first. For the counter 4 xor gates, 4 flip flop and 3 and gates were needed. So And gate and XOR gates were also designed. Then based on these basic gates schematic and layout of the counter was designed.

Test circuitry was designed to check if every gate is working properly. To design the Xor gate, basic NOR gate was designed first. So to build the counter, actually all the basic gates were done first and added to the library. This was very helpful to appreciate modular approach to design in cadence. The schematic and layout of the NAND gate is given below:
Fig: Schematic of the NAND gate.

Fig: Layout of a NAND gate
All the other basic gates were built like this and added to the library for further design of D flipflop and 4 bit counter. The flowchart of the design process is shown below:
**Specification:**

1. AMI 0.6 micron process was used.
2. \(W_p=7.5\mu, W_n=3\mu\) was used. \(L_n=L_p=0.6\mu\) was used.
3. Spectra was used to perform Pre and Post layout simulation.
4. A single clock signal was used for all the flipflops (synchronous counter)

**The Choice of D flip-flop:**

1. It is well suited for integrated circuit application.
2. S-R flipflop has indeterminate state when both inputs are high.
3. The J-K flipflop is better but it has two inputs whereas the D flip flop is much simpler because it has one output.

The truth table for a D flip flop is given below:

<table>
<thead>
<tr>
<th>clk</th>
<th>(Q_{n+1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>(Q_n)</td>
</tr>
<tr>
<td>1</td>
<td>(D)</td>
</tr>
</tbody>
</table>

**Fig: truth table for a D flip flop.**

**Fig: ckt diagram of the master slave D flipflop.**
Fig: Schematic of the D flip flop

Fig: layout of the D flipflop

Fig: symbol of the D flip flop
Design of the synchronous 4 bit counter:

1. Synchronous counter is chosen because it is the most popular type of counter.
2. The propagation delay is comparatively lower than asynchronous counter.
3. Its performance is also better from a reliability perspective because there is no glitch.

![Circuit diagram of the 4 bit synchronous counter](image)

It has 3 AND gates, 4 XOR gates and 4 D Flipflops. Same clock pulse is given to each Flipflop. So with every clock pulse the counter counts one step up. It is a up counter. It starts from 0000. Then with clock pulse counts like 0001, 0010, 0011, 0100 upto 1111. Then it starts from 0000 again. A₀ is the LSB and A₃ is the MSB.

There is a Enable pin. If E=0, then counter Stops counting. IF E=1, each clock pulse results in a counting action. The D flip flop actually works at the rising edge of the clock. But because it is a master slave configuration, it actually stores the input at rising edge and it is given to the output at the falling
edge of the clock. So change in counter output is observed in the falling edge of the clock.
Pre layout simulation output generated from the schematic is given below:

So the design’s effectiveness was verified from this result. After this layout was done and file was extracted from the layout. It passed the DRC check and LVS (Layout vs Schematic test). The simulation result produced from the test counter bench of the extracted file is given below:
Delay Characteristics for Loading effect:

For different capacitive load (1pf-5pf) delay was measured. The graphs of rise time, fall time and propagation delay are given below for all 4 bits of the counter:

**Fig:** Plot of rise time vs load capacitance

Rise time was calculated as the time it takes to get from 0 to 70% of the final value.

Fall time was calculated as the time it takes to come down from 100% to 30% of Vdd.

Propagation delay was measured as the time it takes to make the transition from 50% of input to 50% of output. Here input was the clock signal. The calculator in Cadence was used to measure all these parameters.
As expected with increase in load capacitance, the rise time and fall time increase. Because the RC time constant value increases, delay time increases. The same thing happens for propagation delay as well as is illustrated below:
PAD FRAME implementation:

After completing the land testing with different loading capacitances, I put the layout on the PAD frame for MOSIS fabrication. I made .gds file according to the instructions of the TA and sent it to them. The ultimate layout in the PADFrame with all the protection circuitry is shown below:
Conclusion:

In this project I have learnt how to use cadence to simulate circuitry in a particular process technology. I learnt how to build basic gates in cadence and build on that base to simulate bigger circuits. Creating symbol from schematic, designing the Layout and checking the layout with the schematic to verify if the netlists match were learnt. By including the Set and reset option, this counter design can be improved. In conclusion, I would like to thank the course instructor for providing me with the opportunity of doing this important project and I would also like to thank the TAs for their sincere help.